THE INVENTION CLAIMED IS:

1.   A method of identifying high quality design points in a circuit design comprising:

(a)   defining a plurality of performance specifications for a circuit formed from a plurality of interconnected circuit devices, wherein each performance specification represents a goal for a corresponding performance of the circuit;

(b)   defining at least one device variable for at least one of the circuit devices;

(c)   subject to each device variable and the performance specifications, generating a plurality of design points for the circuit, wherein each design point is comprised of a topology of the circuit devices and the performances associated with said topology;

(d)   for each design point, determining an original cost that is related to the degree of correlation between the performance specifications and the performances of the circuit associated with said design point;

(e)   identifying a subset of said design points;

(f)   for each design point identified in step (e), determining a domination cost as a function of how favorable at least one performance of said design point is with respect to the corresponding performance of at least one other design point identified in step (e);

(g)   for each design point identified in step (e), determining a tradeoff cost by combining the original cost and the domination cost for said design point;

(h)   subject to the performance specifications and the circuit topology associated with each design point of a subset of the identified design points, generating another plurality of design points for the circuit, wherein each thus generated design point is generated from at least one of the subset of the identified design points, and at least one device variable of each thus generated design point has a value that is different than a value of said device variable for the at least one design point from which said thus generated design point was generated;

(i)   for each design point generated in step (h), determining an original cost that is related to the degree of correlation between the performance specifications and the performances of the circuit associated with said design point;

(j)   for each design point generated in step (h), determining a domination cost as a function of how favorable at least one performance of said design point is with respect to the corresponding performance of at least one other design point;

(k)   for each design point generated in step (h), determining a tradeoff cost by combining the original cost and the domination cost for said design point;

(l)   identifying each design point generated in step (h) that has a tradeoff cost that is the same or more favorable than the most favorable tradeoff cost determined before the preceding iteration of step (k); and

(m)   if identifying additional design points is desired, repeating steps (h) through (l).

2.   The method of claim 1, further including:

(n) displaying a subset of the identified design points for selection of one of said identified design points having desired performances for the circuit.

3.   The method of claim 2, wherein, in at least one of step (e), (h) and (n), the subset of design points or identified design point includes all of the design points or identified design points referenced in said step.

4.   The method of claim 1, further including, between steps (k) and (m), for design points generated in step (h) that have tradeoff costs that are less favorable than the most favorable tradeoff cost determined before the preceding iteration of step (k), identifying a subset of said design points utilizing a heuristic.

5.   The method of claim 4, wherein the heuristic includes utilizing a simulated annealing method to identify the subset of design points.

6.   The method of claim 1, wherein the most favorable cost is the lowest cost.

7.   The method of claim 1, wherein determining the domination cost in step (f) includes determining a ratio of:

the total number of design points identified in step (e); and

the number of design points identified in step (e) having at least two more favorable performances than said design point.

8.   The method of claim 1, wherein determining the domination cost in step (f) includes determining a ratio of (1) a distance between at least two performances of said design point and a criteria point representing the smallest or largest permissible values of said two performances and (2) a distance between the criteria point and a tradeoff frontier defined by the other design point.

9.   The method of claim 8, wherein determining the domination cost further includes subtracting said ratio from one (1).

10.   The method of claim 8, wherein said at least two performances of said other design point are more favorable than said at least two performances of said design point.

11.   The method of claim 10, wherein a performance of said one design point is more favorable than a corresponding performance of said other design point when a value of the performance of said one design point is closer to a value of the corresponding performance specification than the value of the performance of said other design point.

12.   The method of claim 1, wherein determining the domination cost in step (j) includes determining a ratio of:

        a sum of the total number of identified design points plus the number of design points generated in step (h); and

        the number of design points of said sum having at least two more favorable performances than said design point.

13.   The method of claim 1, wherein determining the domination cost in step (j) includes determining a ratio of (1) a distance between at least two performances of said design point and a criteria point representing the smallest or largest permissible values of said two performances and (2) a distance between the criteria point and a tradeoff frontier defined by the other design point.

14.   The method of claim 13, wherein determining the domination cost further includes subtracting said ratio from one (1).

15.   The method of claim 13, wherein said at least two performances of said other design point are more favorable than said at least two performances of said design point.

16.   The method of claim 15, wherein a performance of said design point is more favorable than a corresponding performance of said other design point when a value of the performance of said design point is closer to a value of the corresponding performance specification than the value of the performance of said other design point.

17.   The method of claim 1, wherein the subset of design points identified in step (e) are those having most favorable original costs associated therewith.

18.   The method of claim 1, wherein, in step (h), each design point of the subset of identified design points is identified as a function of its tradeoff cost.

19.   The method of claim 1, further including the steps of:
      (aa)   identifying a subset of the identified design points;
      (bb)   processing each design point identified in step (aa) to generate a layout design point that includes a physical layout of the interconnected circuit devices;
      (cc)   processing the physical layout of interconnected circuit devices associated with each layout design point generated in step (bb) to determine layout performances therefor;
      (dd)   determining a tradeoff cost for each layout design point generated in step (bb) that is related to at least one of (1) a degree of correlation between layout performance specifications for the circuit and the layout performances of the physical layout associated with said layout design point and (2) how favorable at least one layout performance of said layout design point is with respect to the corresponding layout performance of at least one other layout design point generated in step (bb);
      (ee)   identifying a subset of said layout design points;

(ff)   generating another plurality of layout design points for the circuit, wherein each thus generated layout design point is generated from at least one of the identified layout design points, and a physical layout associated with each thus generated layout design point is different than the physical layout associated with the at least one identified layout design point from which said thus generated layout design point was generated;

(gg)   processing the physical layout of interconnected circuit devices associated with each layout design point generated in step (ff) to determine layout performances therefor;

(hh)   determining a tradeoff cost for each layout design point generated in step (ff) that is related to at least one of (1) a degree of correlation between the layout performance specifications and the layout performances of the physical layout associated with said layout design point and (2) how favorable at least one layout performance of said layout design point is with respect to the corresponding layout performance of at least one other layout design point;

(ii)   identifying each layout design point generated in step (ff) that has a tradeoff cost that is the same or more favorable than the most favorable tradeoff cost determined before the preceding iteration of step (hh); and

(jj)   if identifying additional layout design points is desired, repeating steps (ff) through (ii).

20.   The method of claim 19, further including, displaying a subset of the identified layout design points for selection of one of said layout design points having desired performances for the circuit.

21.   The method of claim 19, further including, between steps (hh) and (jj), for layout design points generated in step (ff) that have tradeoff costs that are less favorable than the most favorable tradeoff cost determined before the preceding iteration of step (hh), identifying a subset of said layout design points utilizing a heuristic.

22.   A computer readable medium having stored thereon instructions which, when executed by a processor, cause the processor to:

(a)   generate a plurality of design points for a circuit based on at least one predefined performance specification for the circuit and at least one device variable for at least one circuit

device of the circuit, wherein each design point is comprised of a topology of the circuit devices forming the circuit and performances of the circuit associated with said topology;

(b)   determine for each design point an original cost that is related to the degree of correlation between the performance specifications and the performances of the circuit associated with said design point;

(c)   allocate a subset of said design points to a design population;

(d)   for each design point allocated in step (c), determine a domination cost as a function of how favorable at least one performance of said design point is with respect to the corresponding performance of at least one other design point allocated in step (c);

(e)   for each design point allocated in step (c), determine a tradeoff cost by combining the original cost for said design point with the domination cost for said design point;

(f)   subject to the performance specifications and the circuit topology associated with each design point of a subset of the design points allocated to the design population, generate another plurality of design points for the circuit, wherein each thus generated design point is generated from at least one of the design points allocated to the design population, and at least one device variable of each thus generated design point has a value that is different than a value of said device variable for the at least one design point from which said thus generated design point was generated;

(g)   for each design point generated in step (f), determine an original cost that is related to the degree of correlation between the performance specifications and the performances of the circuit associated with said design point;

(h)   for each design point generated in step (f), determine a domination cost as a function of how favorable at least one performance of said design point is with respect to the corresponding performance of at least one other design point;

(i)   for each design point generated in step (f), determine a tradeoff cost by combining the original cost and the domination cost determined for said design point;

(j)   for each design point generated in step (f) that has a tradeoff cost that is the same or more favorable than the most favorable tradeoff cost determined before the preceding iteration of step (i), allocate said design point to the design population; and

(k)   if allocation of additional design points to the design population is desired, repeat steps (f) through (j).

23.   The computer readable medium of claim 22, wherein the instructions further cause the processor to:

        (l) cause a subset of the design points allocated to the design population to be displayed for selection of one of said allocated design points having desired performances for the circuit.

24.   The computer readable medium of claim 23, wherein the subset of design points in at least one of steps (c), (f) and (l) includes all of the design points referenced in said step.

25.   The computer readable medium of claim 22, wherein the instructions further cause the processor to, between steps (i) and (k), for the design points generated in step (f) that have tradeoff costs that are less favorable than the most favorable tradeoff cost determined before the preceding iteration of step (i), allocate a subset of said design points to the design population utilizing a heuristic.

26.   The computer readable medium of claim 25, wherein the heuristic is a simulated annealing method.

27.   The computer readable medium of claim 22, wherein the subset of design points allocated in step (c) are those having most favorable original costs associated therewith.

28.   The computer readable medium of claim 22, wherein the instructions further cause the processor to:

        (aa)   identify a subset of the design points allocated to the design population;

        (bb)   process each design point identified in step (aa) to generate a layout design point that includes a physical layout of the interconnected circuit devices;

        (cc)   process the physical layout of interconnected circuit devices associated with each layout design point generated in step (bb) to determine layout performances therefor;

        (dd)   determine a cost for each layout design point generated in step (bb) that is related to at least one of (1) a degree of correlation between layout performance specifications and the layout performances of the physical layout associated with said layout design point and (2) how favorable at least one layout performance of said layout design point is with respect to the

corresponding layout performance of at least one other layout design point generated in step (bb);

(ee)   allocate a subset of said layout design points to a layout design population;

(ff)   generate another plurality of layout design points for the circuit, wherein each thus generated layout design point is generated from at least one layout design point allocated to the layout design population, and a physical layout associated with each thus generated layout design point is different than the physical layout associated with the at least one layout design point from which said thus generated design point was generated;

(gg)   process the physical layout of interconnected circuit devices associated with each layout design point generated in step (ff) to determine layout performances therefor;

(hh)   determine a cost for each layout design point generated in step (ff) that is related to at least one of (1) a degree of correlation between the layout performance specifications for the circuit layout and the performances of the physical layout associated with said layout design point and (2) how favorable at least one layout performance of said layout design point is with respect to the corresponding layout performance of at least one other layout design point;

(ii)   for each layout design point generated in step (ff) that has a tradeoff cost that is the same or more favorable than the most favorable tradeoff cost determined before the preceding iteration of step (hh), allocate said layout design point to the layout design population; and

(jj)   if allocation of additional layout design points to the layout design population is desired, repeat steps (ff) through (ii).

29.   The computer readable medium of claim 28, wherein the instructions further cause the processor to cause a subset of the layout design points allocated to the design population to be displayed for selection of one of said allocated layout design points having desired performances for the circuit.

30.   The computer readable medium of claim 28, wherein the instructions further cause the processor to, between steps (hh) and (jj), for layout design points generated in step (ff) that have tradeoff costs that are less favorable than the most favorable tradeoff cost determined before the

preceding iteration of step (hh), allocating a subset of said layout design points to the layout design population utilizing a heuristic.

31. A method of identifying high quality design points in a circuit design comprising:

(a) generating a plurality of design points for a circuit based on at least one performance specification for the circuit and at least one device variable for at least one circuit device of the circuit, wherein each design point is comprised of a topology of the circuit devices forming the circuit and performances of the circuit associated with said topology;

(b) allocating a subset of said design points to a design population;

(c) for each allocated design point, determining a cost for said design point as a function of at least one of (1) a degree of correlation between the performance specifications and the performances of the circuit associated with said design point and (2) how favorable at least one performance of said design point is with respect to the corresponding performance of at least one other design point allocated in step (b);

(d) subject to the performance specifications and the circuit topology associated with each design point of a subset of the design points allocated to the design population, generating another plurality of design points for the circuit, wherein each thus generated design point is generated from at least one of the design points allocated to the design population, and each thus generated design point has at least one device variable that has a value that is different than a value of said device variable for the at least one design point from which said thus generated design point was generated;

(e) for each design point generated in step (d), determining a cost for said design point as a function of at least one of (1) a degree of correlation between the performance specifications and the performances of the circuit associated with said design point and (2) how favorable at least one performance of said design point is with respect to the corresponding performance of at least one other design point generated in step (d);

(f) for each design point generated in step (d) that has a cost that is the same or more favorable than the most favorable cost determined before the preceding iteration of step (e), allocating said design point to the design population; and

(g) repeating steps (d) through (f) if additional design points are to be allocated to the design population.

32. The method of claim 31, further including:

(h) displaying a subset of the design points allocated to the design population for selection of one of said allocated design points having desired performances for the circuit.

33. The method of claim 31, further including, between steps (e) and (g), for design points generated in step (d) that have costs that are less favorable than the most favorable cost determined before the preceding iteration of step (e), allocating a subset of said design points to the design population based on a heuristic.

34. The method of claim 33, wherein the heuristic is a simulated annealing method.

35. The method of claim 32, wherein the subset of design points of at least one of steps (b), (d) and (h) includes all of the design points referenced in said step.

36. The method of claim 31, wherein the subset of design points allocated in step (b) are those having most favorable original costs associated therewith.

37. The method of claim 31, further including the steps of:

(aa) identifying a subset of the design points allocated to the design population thus far;

(bb) processing each design point identified in step (aa) to generate a layout design point that includes a physical layout of the interconnected circuit devices;

(cc) processing the physical layout of interconnected circuit devices associated with each layout design point generated in step (bb) to determine layout performances therefor;

(dd) determining a cost for each layout design point generated in step (bb) that is related to at least one of (1) a degree of correlation between layout performance specifications for the circuit and the layout performances of the physical layout associated with said layout design point and (2) how favorable at least one layout performance of said layout design point is with respect to the corresponding layout performance of at least one other layout design point generated in step (bb);

(ee) allocating a subset of said layout design points to a layout design population;

(ff)   generating another plurality of layout design points for the circuit, wherein each thus generated layout design point is generated from at least one layout design point allocated to the layout design population, and a physical layout associated with each thus generated layout design point is different than the physical layout associated with the at least one layout design point from which said thus generated design point was generated;

(gg)   processing the physical layout of interconnected circuit devices associated with each layout design point generated in step (ff) to determine layout performances therefor;

(hh)   determining a cost for each layout design point generated in step (ff) that is related to at least one of (1) a degree of correlation between the layout performance specifications and the layout performances of the physical layout associated with said layout design point and (2) how favorable at least one layout performance of said layout design point is with respect to the corresponding layout performance of at least one other layout design point;

(ii)   for each layout design point generated in step (ff) that has a tradeoff cost that is the same or more favorable than the most favorable tradeoff cost determined before the preceding iteration of step (hh), allocating said layout design point to the layout design population; and

(jj)   if allocation of additional layout design points to the design population is desired, repeat steps (ff) through (ii).

38.   The method of claim 37, further including displaying a subset of the allocated layout design points for selection of one of said allocated layout design points having desired performances.

39.   The method of claim 37, further including, before step (jj), for layout design points generated in step (ff) that have tradeoff costs that are less favorable than the most favorable tradeoff cost determined before the preceding iteration of step (hh), allocating a subset of said layout design points to the layout design population utilizing a heuristic.